## ABSTRACT

An integrated circuit and manufacturing method therefor is provided having a semiconductor substrate with a semiconductor device. A device dielectric layer formed on the semiconductor substrate. A channel dielectric layer on the device dielectric layer has an opening formed therein. A barrier layer lines the channel opening. A conductor core fills the opening over the barrier layer. A cerium-conductor interconnect cap is disposed over the conductor core with a capping layer over the dielectric layer and the cerium-conductor interconnect cap.